

A MEMORY DEVICE WITH AN ALTERNATING V_{ss} INTERCONNECTION

ABSTRACT

A semiconductor memory device provides non-volatile memory with a memory array having an
5 alternating V_{ss} interconnection. Using the alternating V_{ss} interconnection, a low implant dosage is added
to a region proximate to the lower areas of an STI region, such as beneath the STI region, to ameliorate the
problem of low V_{ss} conductivity by providing an adequate number of multiple current paths over several
V_{ss} lines. However, non-adjacent STI regions, rather than adjacent STI region, receive the implant.
Alternating V_{ss} lines are interconnected by thus implanting under every other STI region. This alternating
10 V_{ss} interconnection imparts an adequately high V_{ss} conductivity, yet without diffusion areas merging to
isolate the associated memory device or contaminating the drains and maintains scalability.